Data Sheet | August 24, 2005 | FN2857.7

1 Microsecond Precision Sample and Hold Amplifier

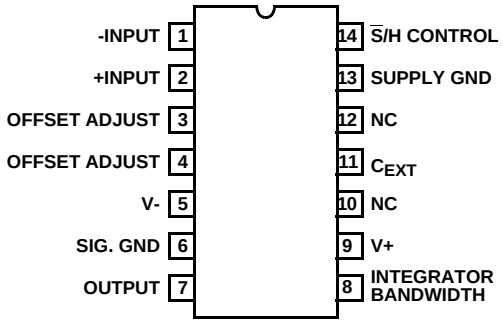
The HA-5320 was designed for use in precision, high speed data acquisition systems.

The circuit consists of an input transconductance amplifier capable of providing large amounts of charging current, a low leakage analog switch, and an output integrating amplifier. The analog switch sees virtual ground as its load; therefore, charge injection on the hold capacitor is constant over the entire input/output voltage range. The pedestal voltage resulting from this charge injection can be adjusted to zero by use of the offset adjust inputs. The device includes a hold capacitor. However, if improved droop rate is required at the expense of acquisition time, additional hold capacitance may be added externally.

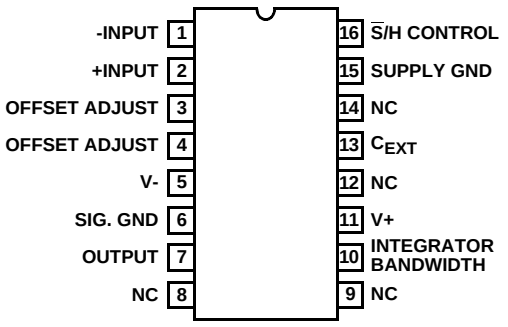
This monolithic device is manufactured using the Intersil Dielectric Isolation Process, minimizing stray capacitance and eliminating SCRs. This allows higher speed and latch-free operation. For further information, please see Application Note AN538.

Pinouts

HA-5320
(PDIP, CERDIP)
TOP VIEW



HA-5320
(SOIC)
TOP VIEW



Features

- Gain, DC . . . . . 2 x 10^6 V/V
- Acquisition Time 1.0µs (0.01%)
- Droop Rate . . . . . 0.08µV/µs (25°C)
  17µV/µs (Full Temperature)
- Aperture Time 25ns
- Hold Step Error (See Glossary) 5mV
- Internal Hold Capacitor
- Fully Differential Input
- TTL Compatible
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

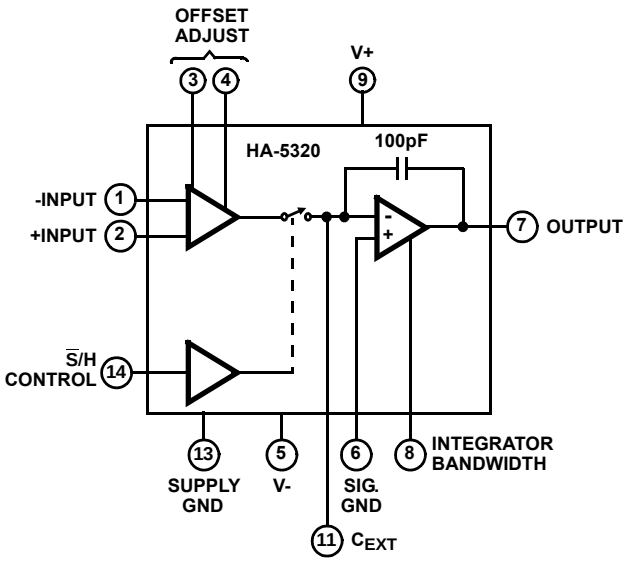
- Precision Data Acquisition Systems
- Digital to Analog Converter Deglitcher
- Auto Zero Circuits
- Peak Detector

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HA1-5320-2	HA1-5320-2	-55 to 25	14 Ld CERDIP	F14.3
HA1-5320-5	HA1-5320-5	0 to 75	14 Ld CERDIP	F14.3
HA3-5320-5	HA3-5320-5	0 to 75	14 Ld PDIP	E14.3
HA9P5320-5	HA9P5320-5	0 to 75	16 Ld SOIC	M16.3
HA9P5320-5Z (Note)	HA9P5320-5Z	0 to 75	16 Ld SOIC (Pb-free)	M16.3

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Functional Diagram



Absolute Maximum Ratings

Supply Voltage 40V
Differential Input Voltage 24V
Digital Input Voltage . . . . . +8V, -15V
Output Current, Continuous (Note 1) . . . . . ±20mA

Operating Conditions

Temperature Range
HA-5320-2 . . . . . -55°C to 125°C
HA-5320-5 . . . . . 0°C to 75°C
Supply Voltage Range (Typical, Note 2) . . . . . ±13.5V to ±20V

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	70	18
PDIP Package	75	N/A
SOIC Package	90	N/A

Maximum Junction Temperature (Ceramic Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Internal Power Dissipation may limit Output Current below 20mA.
2. Specification based on a one time characterization. This parameter is not guaranteed.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ±15.0V; C_H = Internal; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold), Unity Gain Configuration (Output tied to -Input), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5320-2			HA-5320-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Input Voltage Range		Full	±10	-	-	±10	-	-	V
Input Resistance		25	1	5	-	1	5	-	MΩ
Input Capacitance		25	-	-	5	-	-	5	pF
Offset Voltage		25	-	0.2	-	-	0.5	-	mV
		Full	-	-	2.0	-	-	1.5	mV
Bias Current		25	-	70	200	-	100	300	nA
		Full	-	-	200	-	-	300	nA
Offset Current		25	-	30	100	-	30	300	nA
		Full	-	-	100	-	-	300	nA
Common Mode Range		Full	±10	-	-	±10	-	-	V
CMRR	V_{CM} = ±5V	25	80	90	-	72	90	-	dB
Offset Voltage Temperature Coefficient		Full	-	5	15	-	5	20	µV/°C
TRANSFER CHARACTERISTICS									
Gain	DC, (Note 12)	25	10^6	2×10^6	-	3×10^5	2×10^6	-	V/V
Gain Bandwidth Product (A_V = +1, Note 5)	C_H = 100pF	25	-	2.0	-	-	2.0	-	MHz
	C_H = 1000pF	25	-	0.18	-	-	0.18	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage		Full	±10	-	-	±10	-	-	V
Output Current		25	±10	-	-	±10	-	-	mA
Full Power Bandwidth	Note 4	25	-	600	-	-	600	-	kHz
Output Resistance	Hold Mode	25	-	1.0	-	-	1.0	-	Ω
Total Output Noise (DC to 10MHz)	Sample	25	-	125	200	-	125	200	μV_{RMS}
	Hold	25	-	125	200	-	125	200	μV_{RMS}

Electrical Specifications V_{SUPPLY} = ±15.0V; C_H = Internal; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold), Unity Gain Configuration (Output tied to -Input), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5320-2			HA-5320-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
TRANSIENT RESPONSE									
Rise Time	Note 5	25	-	100	-	-	100	-	ns
Overshoot	Note 5	25	-	15	-	-	15	-	%
Slew Rate	Note 6	25	-	45	-	-	45	-	V/µs
DIGITAL INPUT CHARACTERISTICS									
Input Voltage	V_{IH}	Full	2.0	-	-	2.0	-	-	V
	V_{IL}	Full	-	-	0.8	-	-	0.8	V
Input Current	V_{IL} = 0V	25	-	-	4	-	-	4	µA
		Full	-	-	10	-	-	10	µA
	V_{IH} = +5V	Full	-	-	0.1	-	-	0.1	µA
SAMPLE AND HOLD CHARACTERISTICS									
Acquisition Time (Note 7)	To 0.1%	25	-	0.8	1.2	-	0.8	1.2	µs
	To 0.01%	25	-	1.0	1.5	-	1.0	1.5	µs
Aperture Time (Note 8)		25	-	25	-	-	25	-	ns
Effective Aperture Delay Time		25	-50	-25	0	-50	-25	0	ns
Aperture Uncertainty		25	-	0.3	-	-	0.3	-	ns
Droop Rate		25	-	0.08	0.5	-	0.08	0.5	µV/µs
		Full	-	17	100	-	1.2	100	µV/µs
Drift Current	Note 9	25	-	8	50	-	8	50	pA
		Full	-	1.7	10	-	0.12	10	nA
Charge Transfer	Note 9	25	-	0.5	1.1	-	0.5	1.1	pC
Hold Step Error	Note 9	25	-	5	11	-	5	11	mV
Hold Mode Settling Time	To 0.01%	Full	-	165	350	-	165	350	ns
Hold Mode Feedthrough	$10V_{P-P}$, 100kHz	Full	-	2	-	-	2	-	mV
POWER SUPPLY CHARACTERISTICS									
Positive Supply Current	Note 10	25	-	11	13	-	11	13	mA
Negative Supply Current	Note 10	25	-	-11	-13	-	-11	-13	mA
Supply Voltage Range	Note 2		±13.5	–	±20	±13.5	-	±20	V
Power Supply Rejection	V+, Note 11	Full	80	-	-	80	-	-	dB
	V-, Note 11	Full	65	-	-	65	-	-	dB

NOTES:

4. V_O = $20V_{P-P}$; R_L = 2kΩ; C_L = 50pF; unattenuated output.
5. V_O = $200mV_{P-P}$; R_L = 2kΩ; C_L = 50pF.
6. V_O = 20V Step; R_L = 2kΩ; C_L = 50pF.
7. V_O = 10V Step; R_L = 2kΩ; C_L = 50pF.
8. Derived from computer simulation only; not tested.
9. V_{IN} = 0V, V_{IH} = +3.5V, t_R < 20ns (V_{IL} to V_{IH}).
10. Specified for a zero differential input voltage between +IN and -IN. Supply current will increase with differential input (as may occur in the Hold mode) to approximately ±46mA at 20V.
11. Based on a 1V delta in each supply, i.e. 15V $\pm 0.5V_{DC}$.
12. R_L = 1kΩ, C_L = 30pF.

Test Circuits and Waveforms

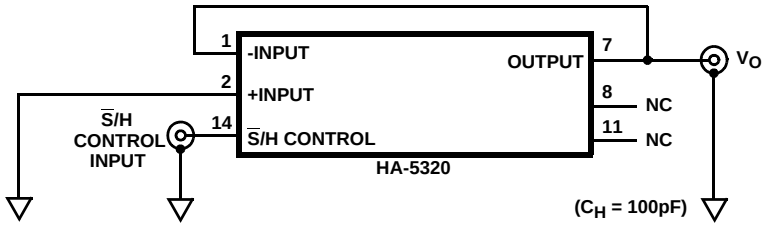
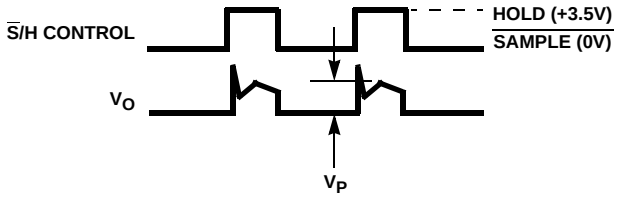


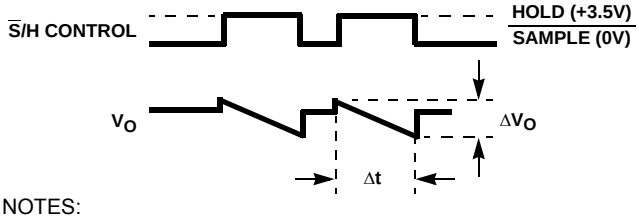
FIGURE 1. CHARGE TRANSFER AND DRIFT CURRENT



NOTES:

13. Observe the "hold step" voltage V_P.
14. Compute charge transfer: $Q = V_P C_H$.

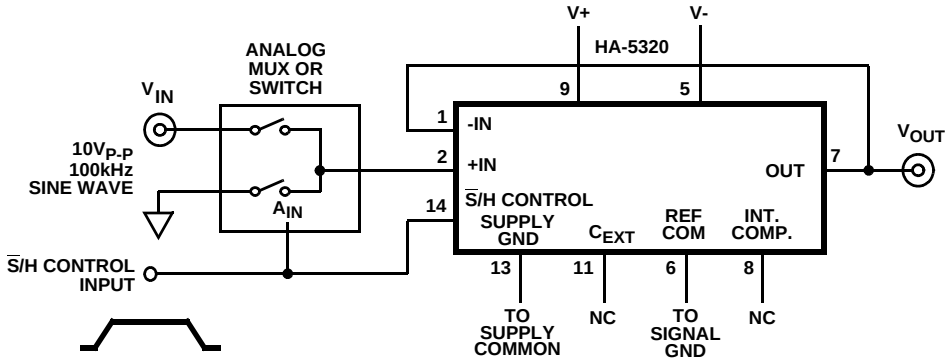
FIGURE 2. CHARGE TRANSFER TEST



NOTES:

15. Observe the voltage "droop", $\Delta V_O/\Delta t$.
16. Measure the slope of the output during hold, $\Delta V_O/\Delta t$, and compute drift current: $I_D = C_H \Delta V_O/\Delta t$.

FIGURE 3. DRIFT CURRENT TEST



NOTE:

Feedthrough in

$$dB = 20\log\frac{V_{OUT}}{V_{IN}}$$ where:

$V_{OUT} = V_{P-P}$, Hold Mode, $V_{IN} = V_{P-P}$.

FIGURE 4. HOLD MODE FEEDTHROUGH ATTENUATION

Application Information

The HA-5320 has the uncommitted differential inputs of an op amp, allowing the Sample and Hold function to be combined with many conventional op amp circuits. See the Intersil Application Note AN517 for a collection of circuit ideas.

Layout

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01μF to 0.1μF, ceramic) should be provided from each power supply terminal to the Supply Ground terminal on pin 13.

The ideal ground connections are pin 6 (SIG. Ground) directly to the system Signal Ground, and pin 13 (Supply Ground) directly to the system Supply Common.

Hold Capacitor

The HA-5320 includes a 100pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Specifications section is based on this internal capacitor).

Additional capacitance may be added between pins 7 and 11. This external hold capacitance will reduce droop rate at the expense of acquisition time, and provide other trade-offs as shown in the Performance Curves.

If an external hold capacitor C_{EXT} is used, then a noise bandwidth capacitor of value $0.1C_{EXT}$ should be connected from pin 8 to ground. Exact value and type are not critical.

The hold capacitor C_{EXT} should have high insulation resistance and low dielectric absorption, to minimize droop errors. Polystyrene dielectric is a good choice for operating temperatures up to 85°C. Teflon® and glass dielectrics offer good performance to 125°C and above.

The hold capacitor terminal (pin 11) remains at virtual ground potential. Any PC connection to this terminal should be kept short and “guarded” by the ground plane, since nearby signal lines or power supply voltages will introduce errors due to drift current.

Typical Application

Figure 5 shows the HA-5320 connected as a unity gain noninverting amplifier - its most widely used configuration. As an input device for a fast successive - approximation A/D converter, it offers very high throughput rate for a monolithic IC sample/hold amplifier. Also, the HA-5320’s hold step error is adjustable to zero using the Offset Adjust potentiometer, to deliver a 12-bit accurate output from the converter.

The application may call for an external hold capacitor C_{EXT} as shown. As mentioned earlier, $0.1C_{EXT}$ is then recommended at pin 8 to reduce output noise in the Hold mode.

The HA-5320 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the S/H output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.

Glossary of Terms

Acquisition Time

The time required following a “sample” command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

Charge Transfer

The small charge transferred to the holding capacitor from the inter-electrode capacitance of the switch when the unit is switched to the HOLD mode. Charge transfer is directly proportional to sample-to-hold offset pedestal error, where: Charge Transfer (pC) = C_H (pF) x Hold Step Error (V)

Aperture Time

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is the interval between the conditions of 10% open and 90% open.

Hold Step Error

Hold Step Error is the output error due to Charge Transfer (see above). It may be calculated from the specified parameter, Charge Transfer, using the following relationship:

$$\text{Hold Step (V)} = \frac{\text{Charge Transfer (pC)}}{\text{Hold Capacitance (pF)}}$$

See Performance Curves.

Effective Aperture Delay Time (EADT)

The difference between the digital delay time from the Hold command to the opening of the S/H switch, and the propagation time from the analog input to the switch.

EADT may be positive, negative or zero. If zero, the S/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

Aperture Uncertainty

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

Drift Current

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D\ (pA) = C_H(pF) \times \frac{\Delta V}{\Delta t}\ (V/s)$$

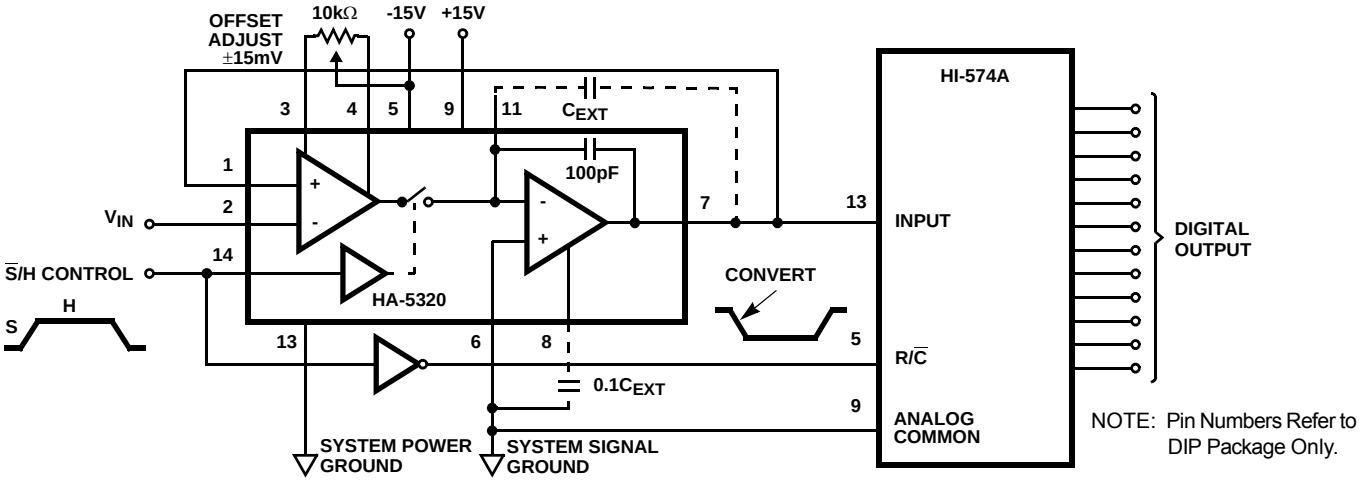


FIGURE 5. TYPICAL HA-5320 CONNECTIONS; NONINVERTING UNITY GAIN MODE

Typical Performance Curves

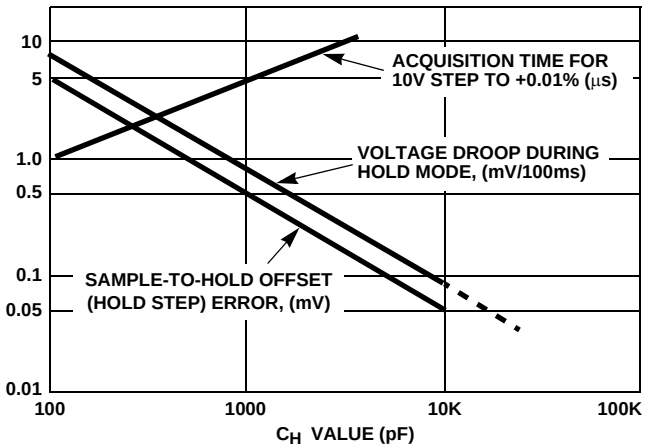


FIGURE 6. TYPICAL SAMPLE AND HOLD PERFORMANCE AS A FUNCTION OF HOLD CAPACITOR

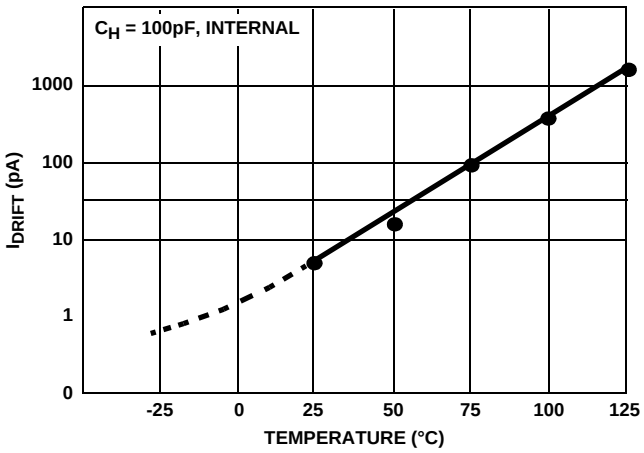


FIGURE 7. DRIFT CURRENT vs TEMPERATURE

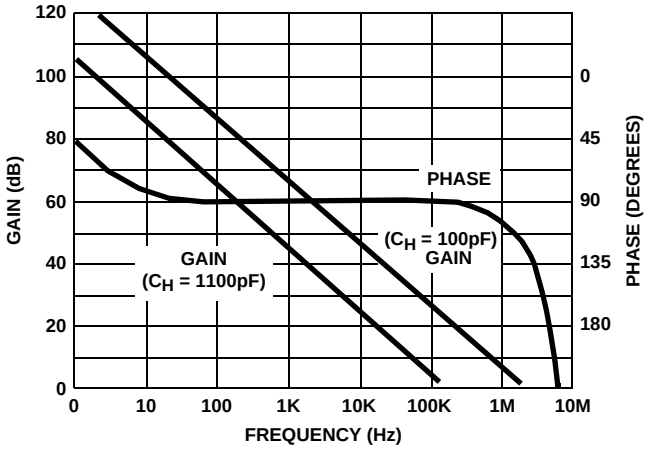


FIGURE 8. OPEN LOOP GAIN AND PHASE RESPONSE

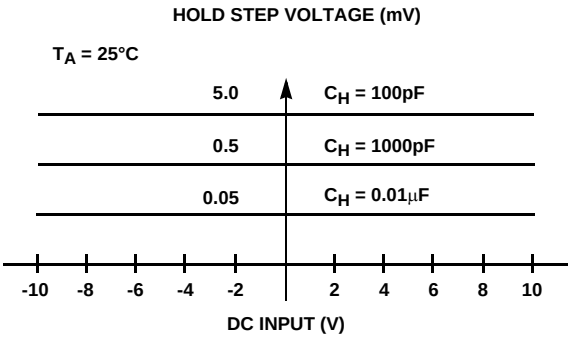


FIGURE 9A. HOLD STEP vs INPUT VOLTAGE

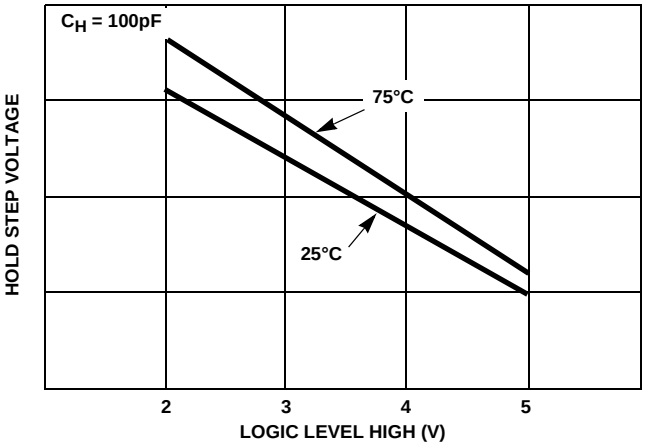


FIGURE 9B. HOLD STEP vs LOGIC (V_{IH}) VOLTAGE

FIGURE 9. TYPICAL SAMPLE-TO-HOLD OFFSET (HOLD STEP) ERROR

Die Characteristics

DIE DIMENSIONS:

92 mils x 152 mils x 19 mils

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

TRANSISTOR COUNT:

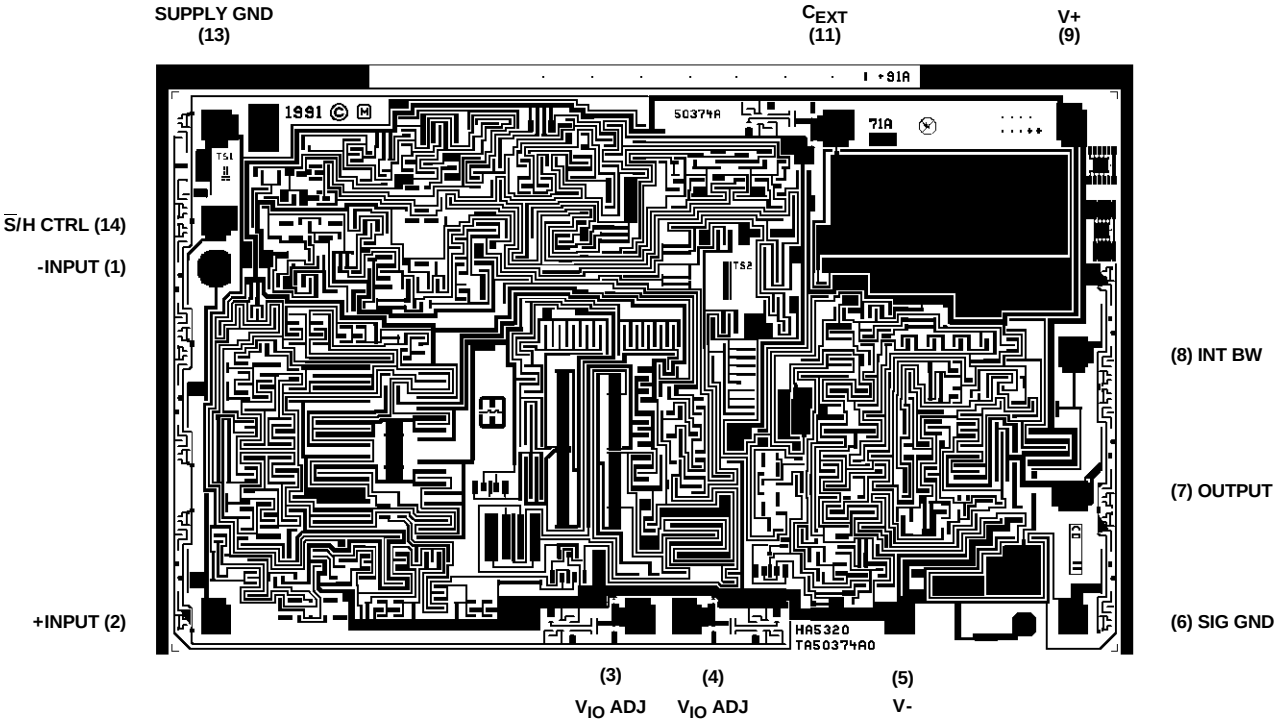
184

SUBSTRATE POTENTIAL:

V-

Metallization Mask Layout

HA-5320



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